400G QSFP-DD FR4 Optical Transceiver (OPDJ02)

Hot Pluggable, Duplex LC,+3.3V, Single mode,EML

Features:

- ✧ QSFP-DD MSA compliant
- ✧ Compliant to 100G Lambda MSA
- ✧ 400G FR4 Specification compliant
- ✧ 4 CWDM lanes MUX/DEMUX design
- ✧ 8x53.125Gb/s PAM4 electrical interface (400GAUI-8)
- ✧ Maximum power consumption 12W
- ✧ LC duplex connector
- ✧ Supports 425Gb/s aggregate bit rate
- ✧ Up to 2km transmission on single mode fiber with FEC
- ✧ Single 3.3V power supply
- ✧ RoHS compliant

Applications

- ✧ 400G Ethernet
- ✧ Data Center Interconnect
- ✧ Enterprise networking

Part Number Ordering Information

OPDJ02	QSFP-DD FR4 2km optical transceiver with full real-time digital diagnostic monitoring and pull tab

1. General Description

OPDJ02 is a transceiver module designed for 2km optical communication applications, and it is compliant to 100G Lambda MSA standard. This module can convert 8-channel 53.125Gb/s electrical data to 4-channel 106.25Gb/s optical signals, and multiplex them into a single channel for 425Gb/s optical transmission. Similarly, it optically de-multiplexes a 425Gb/s input into 4-channel signals, and converts them to 8-channel output electrical data on the receiver side. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

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2. Transceiver Block Diagram

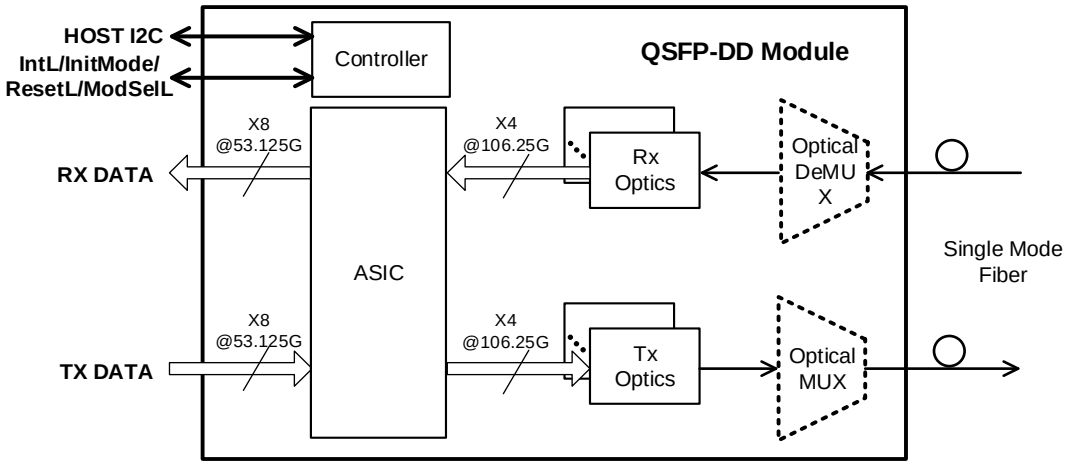

Figure 1. Transceiver Block Diagram

3. Proposed Application Schematics

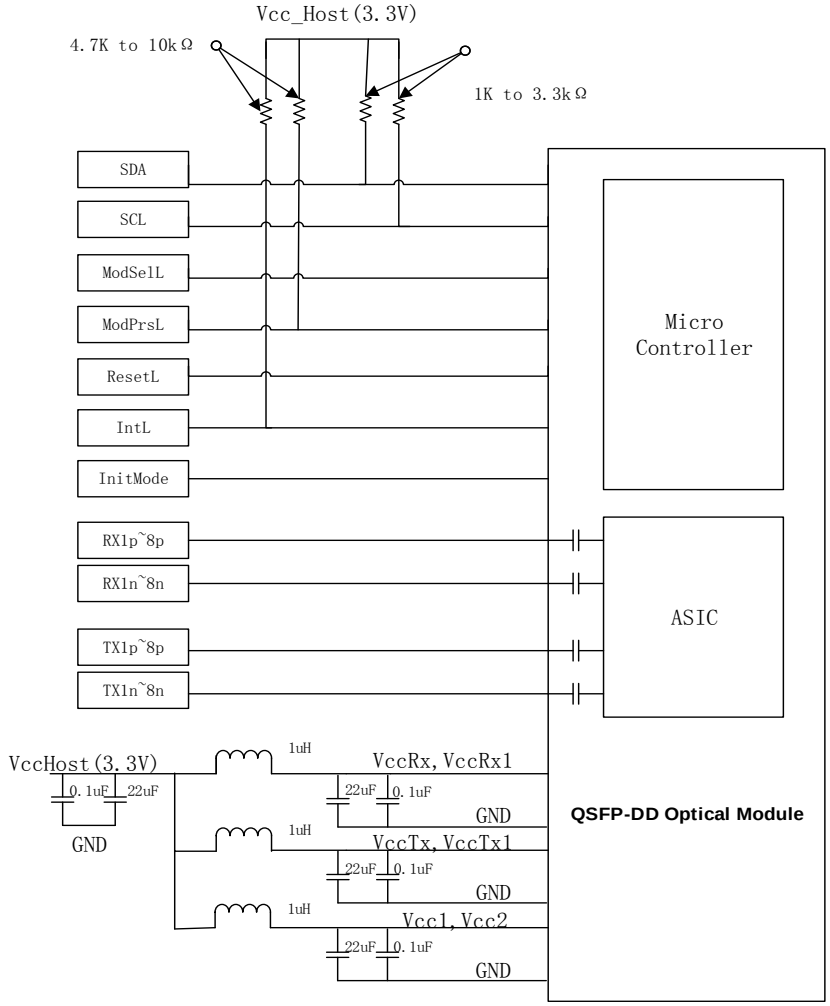

Figure 2. Proposed Application Schematics

4. Pin Descriptions

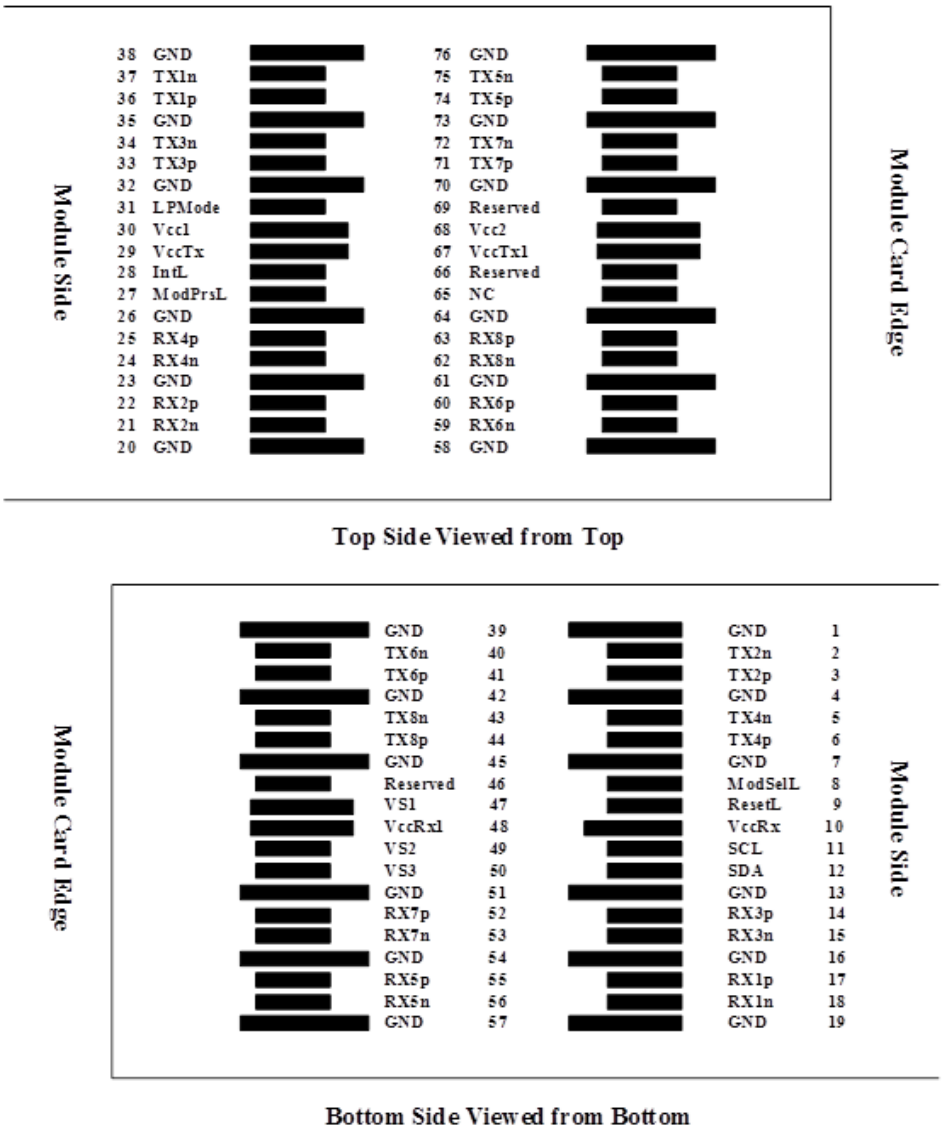

Figure 3. QSFP-DD MSA compliant Connector

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1

8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		Vcc Rx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Non-Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-I	ModPrsL	Module Present	3B	
28	LVTTL-I	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data	3A	

			Input		
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	+3.3V Power supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Out-put	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Out-put	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Non-Inverted Data Out-put	3A	
60	CML-O	Rx6p	Receiver Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Non-Inverted Data Out-put	3A	
63	CML-O	Rx8p	Receiver Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For Future Use	3A	3
67		VccTx1	+3.3V Power supply	2A	2
68		Vcc2	+3.3V Power supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	

76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A,3A,1B,2B,3B. (see Figure 3 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.

5. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum Supply Voltage	Vcc	-0.5	3.3	3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity	RH	0		85	%	

6. Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.135	3.3	3.465	V
Case Temperature	T	0		70	℃
Data Rate Accuracy		-100		100	ppm
Link Distance with G.652				2000	m

7. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power dissipation	P			12	W	
Supply Current	Icc			3.64	A	
Transmitter						
Data Rate, each lane		26.5625±100ppm			GBd	

Differential input Voltage pk-pk	Vpp	900			mV	1
Common Mode Voltage	Vcm	-350		2850	mV	2
Differential Termination Resistance Mismatch				10	%	
Single-ended Voltage Tolerance Range (Min)		-0.4		3.3	V	
Differential Input Return Loss		IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss		IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test		IEEE 802.3bs 120E.3.4.1				3
Receiver						
Data Rate, each lane		26.5625±100ppm			GBd	
Differential Termination Resistance Mismatch				10	%	
Differential output Voltage pk-pk	Vpp			900	mV	
Common Mode Voltage	Vcm	-350		2850	mV	2
Common Mode Noise, RMS	Vrms			17.5	mV	
Transition time (min)		9.5			ps	20%to80%
Near-end Eye height, differential (min)		70			mV	
Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Far-end Eye height, differential (min)		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	dB	
Differential output return loss		IEEE 802.3-2015 Equation (83E-2)				
Common to differential mode conversion return loss		IEEE 802.3-2015 Equation (83E-3)				
Note:						

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.
3. BER specified in IEEE 802.3bs 120E.1.1.

8. Optical Characteristics

Parameters	Unit	min	type	max
Transmitter				
Data Rate, each Lane	GBd	53.125±100ppm		
Modulation Format		PAM4		
Line wavelengths	nm	1264.5	1271	1277.5
		1284.5	1291	1297.5
		1304.5	1311	1317.5
		1324.5	1331	1337.5
Total Average Launch Power	dBm			9.3
Average Launch Power, each lane	dBm	-3.3		3.5
Optical Modulation Amplitude (OMA), each lane	dBm	-0.3		3.7
Extinction Ratio (ER)	dB	3.5		
Side-Mode Suppression Ratio (SMSR)	dB	30		
Launch power in OMA minus TDECQ, each lane, for ER≥4.5dB	dB	-1.7		
Launch power in OMA minus TDECQ, each lane, for ER <4.5dB	dB	-1.6		
Transmitter and Dispersion Eye Clouser for PAM4, each Lane (TDECQ)	dB			3.4
Difference in Launch Power between any Two Lanes (OMAouter)	dB			4
RIN17.1OMA	dB/Hz			-136
Optical Return Loss Tolerance	dB			17.1

Transmitter Reflectance	dB			-26
Average Launch Power of OFF Transmitter, each Lane	dBm			-20
Receiver				
Data Rate, each Lane	GBd	53.125±100ppm		
Modulation Format		PAM4		
Damage Threshold, each lane	dBm	4.5		
Line wavelengths	nm	1264.5		1277.5
		1284.5		1297.5
		1304.5		1317.5
		1324.5		1337.5
Average receiver power, each lane	dBm	-7.3		3.5
Receiver power, each lane (OMA)	dBm			3.7
Difference in Receiver Power between any Two Lanes (OMA)	dB			4.1
Stressed receiver Sensitivity (OMAouter) , each lane(max)	dBm	See Note		
LOS Assert	dBm	-30		
LOS Deassert	dBm			-10
LOS Hysteresis	dB	0.5		
Receiver reflectance	dB			-26
Conditions of Stressed Receiver Sensitivity				
Stressed eye closure for PAM4 (SECQ), lane under test	dB	0.9		3.4
OMAouter of each aggressor lane	dBm		1.5	

Note:
Measured with conformance test signal for BER = 2.4x10-4. A compliant receiver shall have stressed receiver sensitivity (OMA outer), each lane values below the mask of Figure 4, for SECQ values between 0.9 and 3.4 dB.

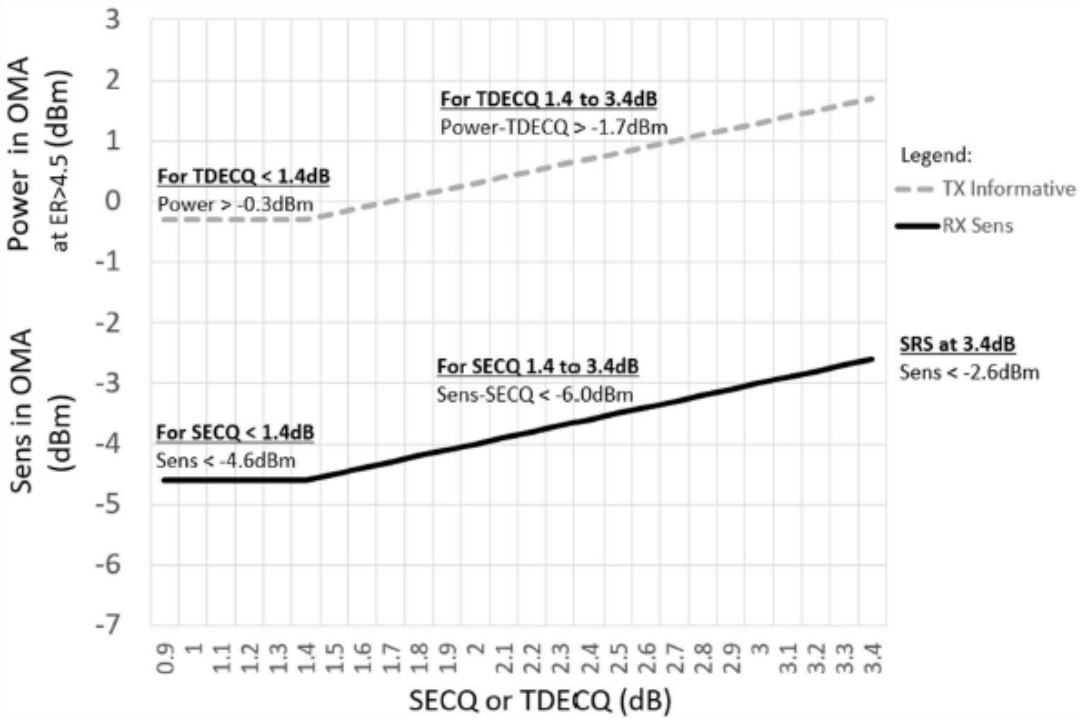

Figure 4. Stressed receiver sensitivity mask for 400G-FR4

9. Digital Diagnostic Monitoring Functions

OPDJ02 support the I2C-based Diagnostic Monitoring Interface (DMI) defined in document SFF-8636. The host can access real-time performance of transmitter and receiver optical power, temperature, supply voltage and bias current.

Performance Item	Related Bytes(A0[00] memory)	Monitor Error	Notes
Module temperature	22 to 23	+/-3°C	1，2
Module voltage	26 to 27	< 3%	2
LD Bias current	42 to 43	< 10%	2
Transmitter optical power	50 to 51	< 3dB	2
Receiver optical power	34 to 35	< 3dB	2

Note

1， Actual temperature test point is fixed on module case around Laser.

2， Full operating temperature range

10. Alarm and Warning Thresholds

OPDJ02 support alarms function, indicating the values of the preceding basic performance are lower or higher than the thresholds.

Performance Item	Alarm Threshold Bytes(A0[03] memory)	Unit	Low thresh-old	High threshold
Temp Alarm	128 to 131	℃	-10	80
Temp Warning	132 to 135	℃	0	70
Voltage Alarm	144 to 147	V	2.97	3.63
Voltage Warning	148 to 151	V	3.135	3.465
TX Power Alarm	192 to 195	dBm	-6.3	6.5
TX Power Warning	196 to 199	dBm	-3.3	3.5
RX Power Alarm	176 to 179	dBm	-10.6	6.5
RX Power Warning	180 to 183	dBm	-7.6	3.5

11. Mechanical Specifications

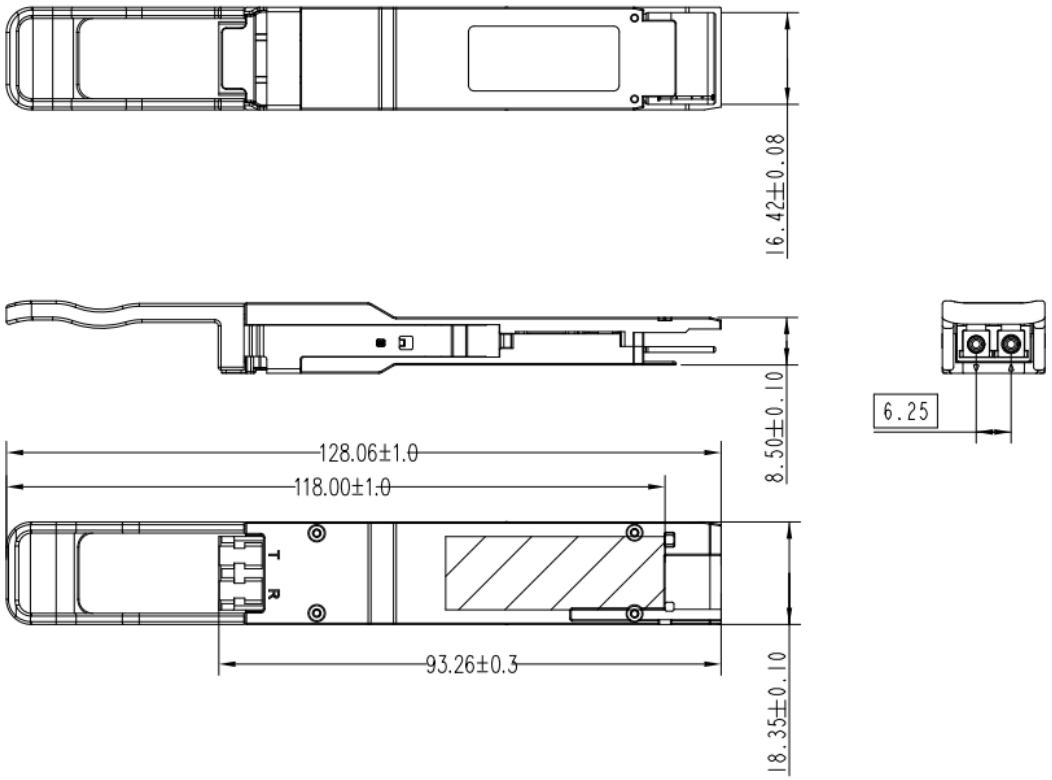

Figure 5. OPDJ02 Mechanical Dimensions

12. Regulatory Compliance

OPDJ02 Optical Transceiver is RoHS 6/6 compliant and complies with international electro-magnetic compatibility (EMC) and product safety requirements and standards.

Feature	Standard	Performance
Safety		
UL	UL 62368-1	UL recognized component for US and CAN
	CAN/CSA C22.2 No. 62368-1-14	
TUV	EN 60950-1	TUV certificate
	EN/IEC 60825-1:2007,Edition 2	
	EN/IEC 60825-1:2014,Edition 3	
	EN/IEC 60825-2:2004+A1:2006+A2:2010	
FDA	U.S. 21 CFR 1040.10	FDA/CDRH certified with ac-ces-sion number according to Laser Notice 50
Electromagnetic Compatibility		
Radiated emis-sions	EMC Directive 2014/30/EU	Class B digital device with a minimum -6dB margin to the limit when tested with a metal enclo-sure. Final margin may vary de-pending on system ap-plication, good system EMI de-sign practice, ie: suitable metal enclosure and well-bonding, is required to achieve Class B margins at the system level. Tested frequency range: 30 MHz to 40 GHz or 5th harmonic (5 times the highest frequency), whichever is less.
	EN 55032	
	CISPR 32	
	FCC rules 47 CFR Part 15	
	ICES-003	
	AS/NZS CISPR 32	
ESD	EN 55024	Withstands discharges of ± 8 k V contact, ±15 k V air.
	CISPR 24	
	IEC/EN 61000-4-2	
Radiated im-	EN 55024	Field strength of 10 V/m from

munity	CISPR 24	80 MHz to 6 GHz.
	IEC/EN 61000-4-3	
Restriction of Hazardous Substances		
RoHS	EU Directive 2011/65/EU (EU) 2015/863	

13. ESD Design

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Parameter	Threshold value	Notes
ESD of high-speed pins	1KV	Human Body Model
ESD of low-speed pins	2KV	Human Body Model
Air discharge during operation	15KV	
Direct contact discharges to the case	8KV	