Features:

- ✧ Compliant with QSFP-DD MSA Specification Rev 3.4;
- ✧ SFF-8679 electrical interface compliant;
- ✧ SFF-8636 management interface support;
- ✧ Support 25G NRZ electrical data rates/channel;
- ✧ I2C for EEPROM communication；Pull to Release latch design;
- ✧ Excellent EMI/EMC performance 360 degree cable shield termination;
- ✧ Advantage dual side pre-solder automated assembly technologies；
- ✧ Low loss, stronger mechanical features, more flexible；
- ✧ QSFP-DD modules will be backwards compatible, allowing them to support existing QSFP modules and provide flexibility for end users and system designers；

Applications:

- ✧ Data center & Networking Equipment
- ✧ Servers/Storage Devices
- ✧ High Performance Computing (HPC)
- ✧ Switches/Routers

Standards Compliance

- ✧ IEEE802.3Bj,IEEE802.3CD
- ✧ RoHS Complia

● Ordering information

Part Number	SPEED	Specifications			Categories
		Length(mm)	Gauge(awg)	Tolerance (mm)	
OPDHT0.5	200G	0.5	30	±15	QSFP-DD TO QSFP-DD
OPDHT1	200G	1.0	30	±25	
OPDHT1.5	200G	1.5	30	±30	
OPDHT2	200G	2.0	28	±35	
OPDHT2.5	200G	2.5	28	±35	
OPDHT3	200G	3.0	26	±45	

● Product Description:

In an effort to keep up with the demands of higher performance and increasing amounts of memory bus bandwidth, OPWAYdesigners are working to revise, extend and update the solution. OPWAY 200G QSFP-DD passive cable assembly can provide new generation performance of QSFP by higher date transfer rate. At the same time, OPWAY QSFP-DD cable choose dual side drain cable and self-designed PCBA, provide low loss， less skew and better NEXT. 360 degree EMI crimping

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shielding and Zinc Die-cast shell designing make the product high-performance. And all the designing is based on the industry standard specifications, such as SFF-8679, SFF-8636 and QSFP-DD MSA specification rev 4.0.

- **Schematic:**

WIRING TABLE----QSFP-DD TO QSFP-DD

P1		P2	
GND(TX)	P1	P20	GND(RX)
TX2n	P2	P21	RX2n
TX2p	P3	P22	RX2p
GND(TX)	P4	P23	GND(RX)
TX4n	P5	P24	RX4n
TX4p	P6	P25	RX4p
GND(TX)	P7	P26	GND(RX)
GND(RX)	P13	P32	GND(TX)
RX3p	P14	P33	TX3p
RX3n	P15	P34	TX3n
GND(RX)	P16	P35	GND(TX)
RX1p	P17	P36	TX1p
RX1n	P18	P37	TX1n
GND(RX)	P19	P38	GND(TX)
GND(RX)	P20	P1	GND(TX)
RX2n	P21	P2	TX2n
RX2p	P22	P3	TX2p
GND(RX)	P23	P4	GND(TX)
RX4n	P24	P5	TX4n
RX4p	P25	P6	TX4p
GND(RX)	P26	P7	GND(TX)
GND(TX)	P32	P13	GND(RX)
TX3p	P33	P14	RX3p
TX3n	P34	P15	RX3n
GND(TX)	P35	P16	GND(RX)
TX1p	P36	P17	RX1p
TX1n	P37	P18	RX1n
GND(TX)	P38	P19	GND(RX)
SHELL		SHELL	

P1		P2	
GND(TX)	P39	P58	GND(RX)
TX6n	P40	P59	RX6n
TX6p	P41	P60	RX6p
GND(TX)	P42	P61	GND(RX)
TX8n	P43	P62	RX8n
TX8p	P44	P63	RX8p
GND(TX)	P45	P64	GND(RX)
GND(RX)	P51	P70	GND(TX)
RX7p	P52	P71	TX7p
RX7n	P53	P72	TX7n
GND(RX)	P54	P73	GND(TX)
RX5p	P55	P74	TX5p
RX5n	P56	P75	TX5n
GND(RX)	P57	P76	GND(TX)
GND(RX)	P58	P39	GND(TX)
RX6n	P59	P40	TX6n
RX6p	P60	P41	TX6p
GND(RX)	P61	P42	GND(TX)
RX8n	P62	P43	TX8n
RX8p	P63	P44	TX8p
GND(RX)	P64	P45	GND(TX)
GND(TX)	P70	P51	GND(RX)
TX7p	P71	P52	RX7p
TX7n	P72	P53	RX7n
GND(TX)	P73	P54	GND(RX)
TX5p	P74	P55	RX5p
TX5n	P75	P56	RX5n
GND(TX)	P76	P57	GND(RX)
SHELL		SHELL	

Cable Assembly Characteristics

QSFP-DD TO QSFP-DD

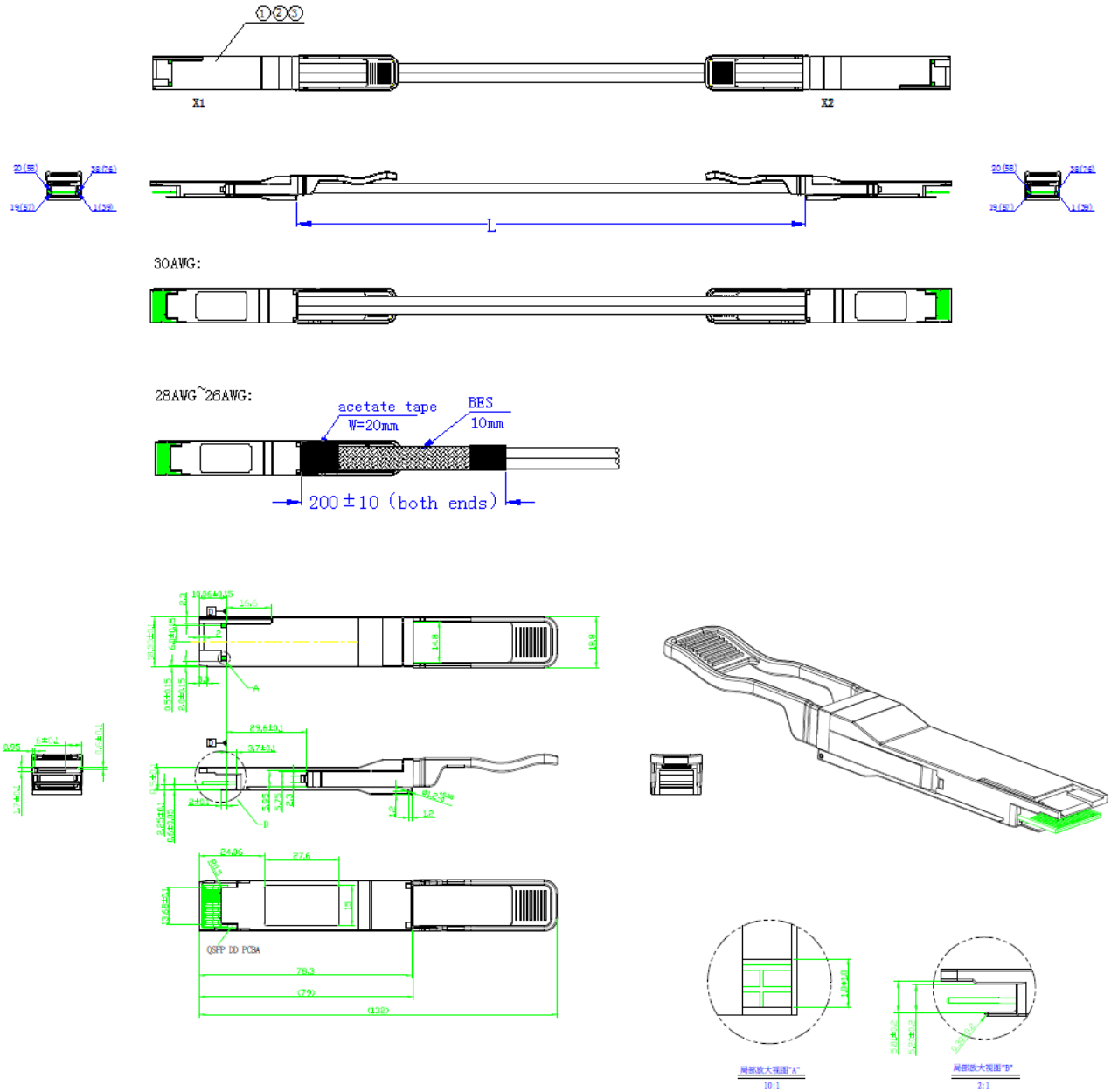


Figure 1 QSFP-DD TO QSFP-DD Mechanical Structure

Electrical Design

The electrical design of the QSFP-DD cable assembly is fully compliant to QSFP-DD Hardware Rev4.0 specifications. The electrical design included: a low loss design printed circuit board, DC block capacitances in the Rx channel, and EEprom chips for the management. Pin layout and function definition are shown in Figure 2 and Table 1.

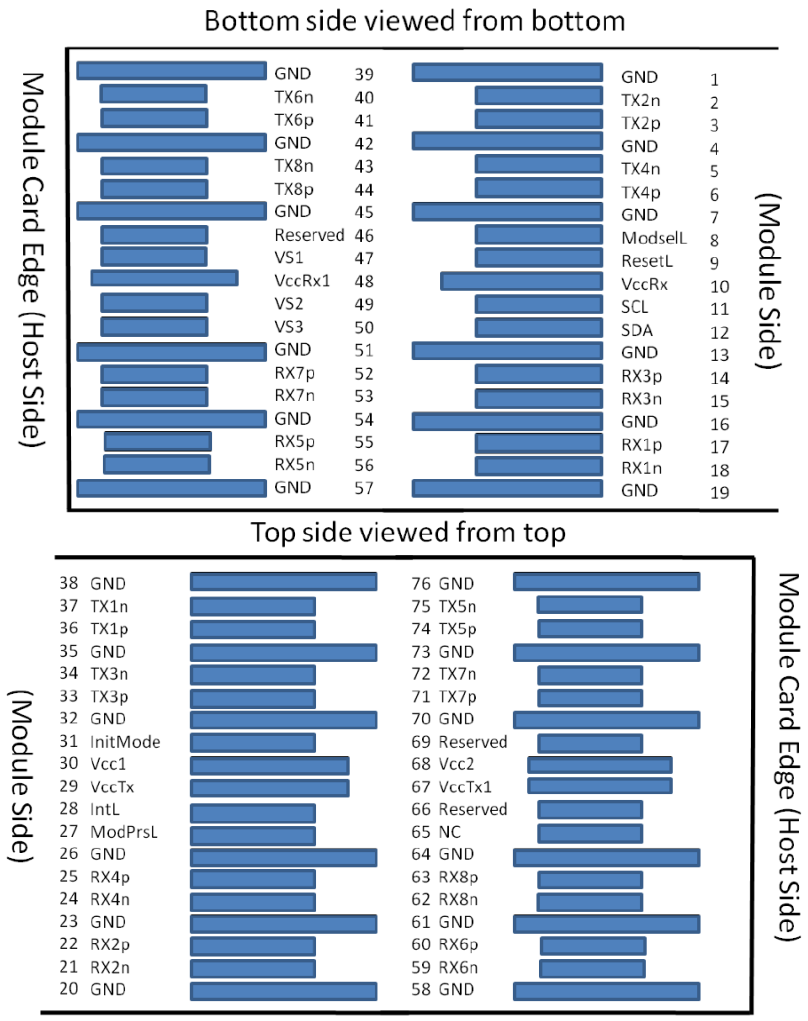


Figure 2 QSFP-DD Pin Define

Table 1 QSFP-DD Pin Function Definition

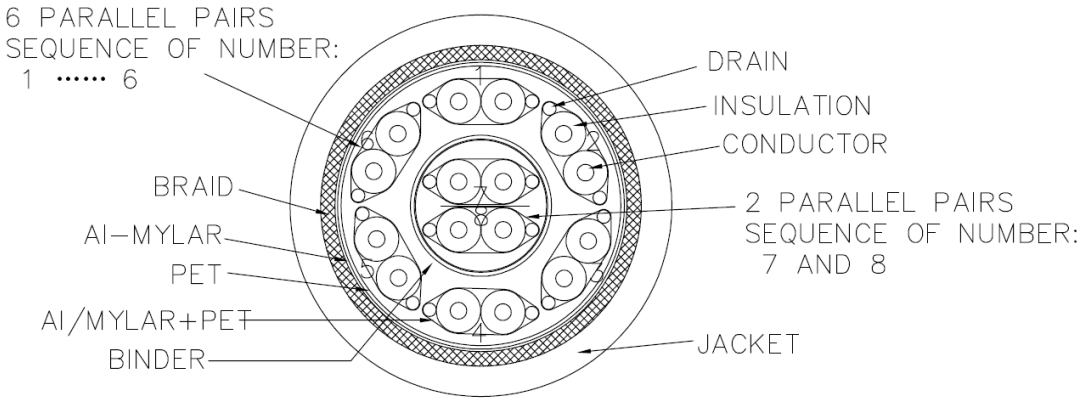
Pin	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	

18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vccl	+3.3V Power Supply	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VSl	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	

63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1
Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.				
Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.				
Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.				
Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.				

● Bulk Cable Characteristics

The structure of the cable is shown as the figure , the characteristics of the bulk cable are listed below.



SECTIONAL DRAWING:

✧ Voltage rating: 30V

- ✧ Temperature rating: 80℃;
- ✧ Impedance: Differential mode: 100 +5/-5 ohm @TDR;
- ✧ Delay Skew(INTRA-SKEW): 30ps/5m max;
- ✧ Signal Twin-ax pair cable: Solid Ag plated copper conductor;
- ✧ Braid shielding coverage 85% min.
- ✧ Jacket material: PVC

● Qualification Requirement Characteristics

<table>
<tr><th colspan="2">ITEM</th><th>REQUIREMENT</th><th>TEST CONDITION</th></tr>
<tr><td rowspan="3">Differential Impedance</td><td>Cable Impedance</td><td>105+5/-10Ω</td><td rowspan="3">Rise time of 25ps (20 % - 80 %).</td></tr>
<tr><td>Paddle Card Impedance</td><td>100±10Ω</td></tr>
<tr><td>Cable Termination Impedance</td><td>100±15Ω</td></tr>
<tr><td colspan="2">Differential (Input/Output)Return loss S_{DD11}/S_{DD22}</td><td>$\begin{cases} 16.5-2\sqrt{f} & 0.05 \leqslant f < 4.1 \\ 10.66-14\log_{10}(f/5.5) & 4.1 \leqslant f \leqslant 19 \end{cases}$</td><td>10MHz≤f ≤19GHz</td></tr>
<tr><td colspan="2">Differential to common-mode (Input/Output)Return loss S_{CD11}/S_{CD22}</td><td>$\begin{cases} 22-(20/25.78)f & 0.01 \leqslant f < 12.89 \\ 15-(6/25.78)f & 12.89 \leqslant f \leqslant 19 \end{cases}$</td><td>10MHz≤f ≤19GHz</td></tr>
<tr><td colspan="2">Common-mode to Common-mode (Input/Output)Return loss S_{CC11}/S_{CC22}</td><td>$Return\_loss(f) \geqslant 2dB \quad 0.2 \leqslant f \leqslant 19$
Where is the frequency in GHz
Return_loss(f) is the common-mode to common-mode return loss at frequency f</td><td>10MHz≤f ≤19GHz</td></tr>
<tr><td colspan="2">Differential Insertion Loss (S_{DD21} Max.)</td><td><table><tr><th>F
AWG</th><th>1.25GHz</th><th>2.5GHz</th><th>5.0GHz</th><th>7.0GHz</th><th>10Ghz</th><th>12.89Ghz</th></tr><tr><td>30(1m) Max.</td><td>4.5dB</td><td>5.4dB</td><td>6.3dB</td><td>7.5dB</td><td>8.5dB</td><td>10.5dB</td></tr><tr><td>30/28(3m)Max.</td><td>7.5dB</td><td>9.5dB</td><td>12.2dB</td><td>14.8dB</td><td>18.0dB</td><td>21.5dB</td></tr><tr><td>26(3m) Max.</td><td>5.7dB</td><td>7.2dB</td><td>9.9dB</td><td>11.9dB</td><td>14.1dB</td><td>16.5dB</td></tr></table></td><td>10MHz≤f ≤19GHz</td></tr>
<tr><td colspan="2">Differential to common-mode Conversion Loss-Differential Insertion Loss(S_{CD21}-S_{DD21})</td><td>$\begin{cases} 10 & 0.01 \leqslant f < 12.89 \\ 27-(29/22)f & 12.89 \leqslant f < \end{cases}$</td><td>10MHz≤f ≤19GHz</td></tr>
<tr><td colspan="2">MDNEXT(multiple disturber near-end crosstalk)</td><td>≥26dB @12.89GHz</td><td>10MHz≤f ≤19GHz</td></tr>
</table>

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